ABSTRACT

An integrated circuit (IC) with high electron mobility transistors, such as enhancement mode pseudomorphic high electron mobility transistors (E-pHEMTs) and method for fabricating the IC utilizes an increased gate-to-drain etch recess spacing in some of the high electron mobility transistors to provide on-chip electrostatic discharge protection. The use of the increased gate-to-drain etch recess spacing allows smaller high electron mobility transistors to be used for ancillary low speed applications on the IC, which reduces the chip area occupied by these ancillary transistors.